Real-Time DSP Data Acquisition System

Steve Connors, Data Translation, Marlboro, Massachusetts

The architecture of a data acquisition system utilizing the processing capability of a DSP chip has existed for many years. The ability to do this in a local loop in real time is available today with chips such as the Texas Instruments'[1] floating-point TMS320C6711. There are many advantages of such an approach for real-time processing. Also of great interest is the ability for users to stream fast data rates to a host in an economical way. The new standard of USB[2] 2.0 allows high speed data transfer between such a DSP peripheral or standalone and a host PC.

If such a DSP-based data acquisition system could use the highest accuracy currently available and still transfer data at rates up to 480 Mbps, it would be quite a breakthrough. Current relative accuracy limits for data acquisition are 24-bit or 60 ppb (parts per billion). The challenge is to combine this with data rates as high as 100,000 measurements per second. A system architect could use such performance either in a local control loop or on a stream basis via the USB 2.0 communications link. This freedom of choice would solve many measurement challenges in industrial systems. For example, such an embedded system could perform signal processing and real-time control independently of the host or under the control of the host processor.

Other key advantages of this type of system would be:

- Plug & play features of USB 2.0, which allow quick and easy setup of the data acquisition system.
- Galvanic isolation could be implemented to protect the host computer from ground loops and voltage transients – a capability not often found on data acquisition products. Galvanic isolation also helps adhere to the tough CE requirements of EN50082-1:1998.
- Programs can be downloaded via USB 2.0 to on-board memory or flash.

Ideally, this data acquisition system would allow simultaneous operation in real-time of all measurement subsystems at high throughput rates and at high accuracy. The TMS320C6711 floating-point DSP could read data from 24-bit sigma delta A/Ds, write data to 24-bit sigma-delta D/As, do digital input/output control operations, or use on-board 32-bit up/down counter timers, all simultaneously and in real-time. Scalability of these operations would also be possible by adding system boards with common clocks and triggers. Data would be either sent to the host using USB 2.0 or shared between processes with on-board 50 MB per second LVDS ports. An additional benefit of the USB 2.0 communication mechanism would be power or system operation availability as part of the connector mechanism.

Introduction. Data Translation has designed such a system, the DT9841 Fulcrum® II Series. This article outlines the design considerations and trade-offs made. To begin with, the on-board subsystems are:

- USB 2.0 for connectivity to a host computer
- 100 kHz, 24 bit analog to digital conversion
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- 24 lines digital input/output
- 32 bit counter timers
- 150 MHz floating point DSP processor
- 50 Mb per second LVDS port for connectivity between modules

USB 2.0 provided the standard high-speed connectivity to numerous computers at speeds up to 480 Mbits per second for downloading programs to the DSP processor and reporting or streaming data back to the host computer. The selected processor was an 8-bit machine with an integrated state machine to independently move data through FIFOs to and from the USB pipes. The USB processor also does double duty in controlling the interface through the galvanic isolation barrier to the DSP chip.

The TMS320C6711 was chosen for the DSP engine because of numerous hardware considerations in addition to the standard software tools available today. The Host Port Interface on the DSP provides a standard, high-speed interface to the USB processor for sending and receiving data. A feature not so obvious is that it is under control of the USB processor on boot up. This allows programs to be downloaded from the host PC to the DSP processor on power up. Another option would be to allow stand-alone operation with the boot-up from the on-board 2 Mb flash memory.

A CPLD (Complex Programmable Logic Device) was used as the glue logic on the USB side of the isolation barrier because it operates on lower power and powers up already programmed and ready to go. On the DSP side of the isolation barrier an FPGA (Field Programmable Gate Array) is used for the glue logic. All sub-system data are passed to and from the DSP processor through the FPGA. This allowed for maximum flexibility in the current design and opens a wide range of options for the future, including preprocessing of the data being input to the front of the DSP.

Signal integrity is paramount in any high performance data acquisition system, especially at 24 bits of analog resolution and 100 kHz conversion rates all on the same board with 150 MHz clocks and high speed processing. Standard plug-in modules were also considered, but given the high frequency clocking on-board and the switching power supplies that were used in order to keep the heat down, we decided to use cold rolled steel cases to enclose and shield the analog circuits. These modules provide both electrostatic and electromagnetic shielding to all the critical analog functions. In addition the PC board is divided into several areas with power plane splits dividing the sub-systems in order to minimize cross talk between the analog and digital subsystems.

Considering both signal integrity and the often harsh industrial environment, it was determined that galvanic isolation was a necessity. This type of isolation completely separates the grounds of the host computer system from all the I/O subsystems. The isolation barrier breakdown voltage must be greater than local line voltage in case of an inadvertent connection. On the signal integrity side, this type of isolation also prevents even microamperes of ground loop current that can cause errors in high resolution analog systems.

Sigma-delta A/D and D/A converters were chosen to minimize the customer's signal conditioning requirements. The on-board filtering provided by this technology removes the need for external anti-alias filters in most applications. This does introduce some delay between the time an analog signal changes and the digital output. This delay is referred to as the "group delay" and is predictable with the following expression for the A/D, Group Delay=37/FS. FS is the selected clock rate of the A/D converter, 370 microseconds at 100 kHz throughput. As it turns out this is almost the same delay that would be introduced by an analog anti-alias filter.

Low Voltage Differential Signal (LVDS) devices for the external data path enabled the sharing of data among multiple boards for processing and stimulus to a wide range of vibration applications. This provided not only speed and signal integrity, but also low noise for passing the EMI requirements. This is yet another area where the glueless interfaces of the TMS320C6711 were utilized, using a slower write setting than read when the LVDS subsystem chip is enabled. This insures that the FIFO on the receiving module does not overflow, even taking into consideration the latency of the interrupt service routine.

Starting the Subsystems. Once the program is loaded the subsystems can be started with an internal or external trigger and clocked with an internal or external clock for synchronization. This highlights another hardware consideration in the selection of the TMS320C6711. Interrupts from the subsystems are dedicated to the servicing and movement of real-time data under DMA control. For ex-

ample, Interrupt 5 would initiate a DMA transfer to output another point of data to the on-board D/A converters or Interrupt 6 would initiate a DMA transfer to collect another data sample from an A/D converter or even do a simultaneous snap of all eight A/D converters along with all counter values and digital inputs. This all takes place in the background while the DSP chip is performing calculations or moving results up to the host computer through the USB 2.0 interface.

Firmware. The firmware and operating system are loaded on power-up through the USB 2.0 interface from the host computer to the memory on the DSP side of the board. The USB controller holds the DSP processor in reset until the memory is loaded. When the reset line is released the DSP program starts. Once started, one of the TMS320C6711 timers is used to interrupt the processor to check for commands from the host or let the host know that there are data ready. A key feature here is that a bit is set and reset each time the counter loops, allowing for a heart beat to be monitored by the host, insuring the process is still running. This heartbeat signal is also divided down to drive a LED on the front panel for a quick indicator for the operator. In addition the on-board firmware can be set to run stand-alone, placing critical data into flash memory if communication is lost to the host.

Debug. A JTAG port has been provided for debug and software development using standard tools such as the Blackhawk emulator and Code Composer. A second key feature that is not included in the block diagram is a bank of eight LEDs on the board that are memory mapped through the FPGA so that a programmer can set and reset up to 255 visible flags in hardware as the program progresses. This way even if the program locks up the LED flags will give a quick hardware indication of the particular function being processed at that time.

Regulatory. Consideration for harsh industrial environments and the tough FCC and CE requirements must be done early in the design cycle. Galvanic isolation to the host computer along with a hand optimized multi-layer printed circuit board design are key to meeting these requirements. This is above and beyond the normal resistor/diode transient protection on all the I/O lines.

User Friendly. On initial set-up, the Plug & Play capability of USB 2.0 allows the user to get the DT9841 module up and running quickly, downloading and executing example programs to the DSP. Calibration is software controlled and saved in onboard, non-volatile memory. Additionally, setup information such as LVDS termination resistors and analog input bias return resistors are also software programmable and stored in onboard non-volatile memory. Thinking about the final package, depending on how many modules are in a system and the enclosure used, we also took into consideration the heat rise. There is a bit in a register to warn if the temperature exceeds 60° C. There is also a FET switch connected to a plug to switch on a low power fan for cooling if the temperature exceeds 45° C.

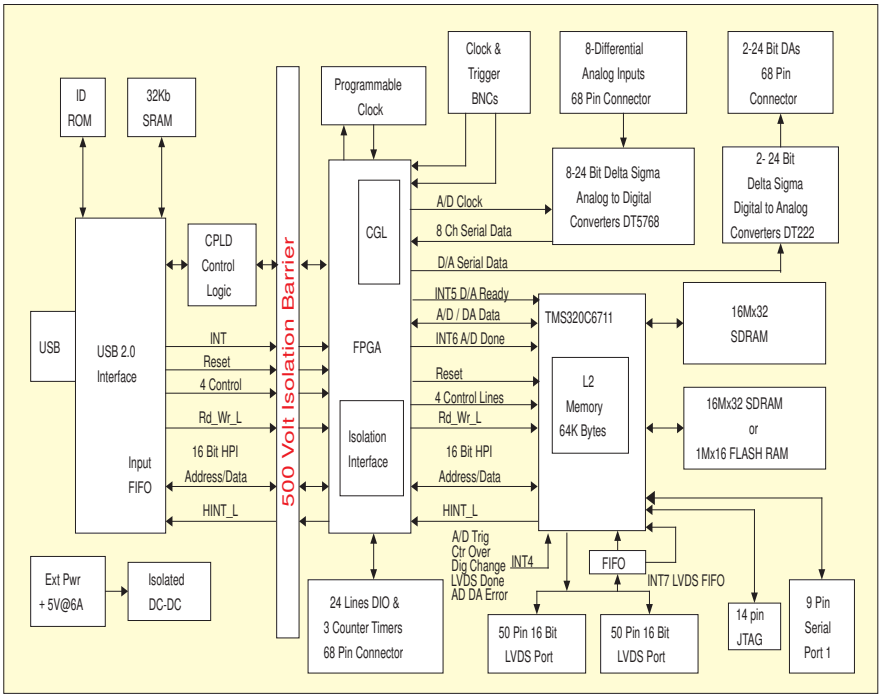

Figure 1. Functional block diagram of the DT9841 Fulcrum II Series data acquisition card.

Summary. This confluence of system architecture components will allow high-speed performance at low-cost in a standard system configuration. Users who need to do real-time data acquisition would benefit by the combination of the high-speed performance capabilities available today with the ability to transfer data to and from the host PC at high data rates. The performance of a floating point chip such as the TI 6711 allows accurate real time processing of signals in a system configuration that would be of great benefit to the user.

Figure 2. DT9841 Fulcrum II Series with TI C6711 floating-point DSP.

1. Texas Instruments' Website: www.ti.com.
2. USB Website: www.usb.org.

The author can be contacted at: sconnors@datx. com.